

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
17 February 2005 (17.02.2005)

PCT

(10) International Publication Number
WO 2005/015188 A1

(51) International Patent Classification⁷: G01N 21/956,
G12B 21/02, 21/22

(72) Inventor; and
(75) Inventor/Applicant (for US only): KUNIMUNE, Yori-
nobu [JP/JP]; c/o NEC Electronics Corporation, 1753 Shi-
monumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-
8668 (JP).

(21) International Application Number:
PCT/JP2003/012389

(22) International Filing Date:
29 September 2003 (29.09.2003)

(74) Agent: FUJIMAKI, Masanori; 5th Floor, Fukoku
Seimei Building, 2-2, Uchisaiwaicho 2-chome, Chiyo-
oda-ku, Tokyo 100-0011 (JP).

(25) Filing Language: English

(81) Designated States (national): CN, KR, US.

(26) Publication Language: English

(84) Designated States (regional): European patent (DE, FR).

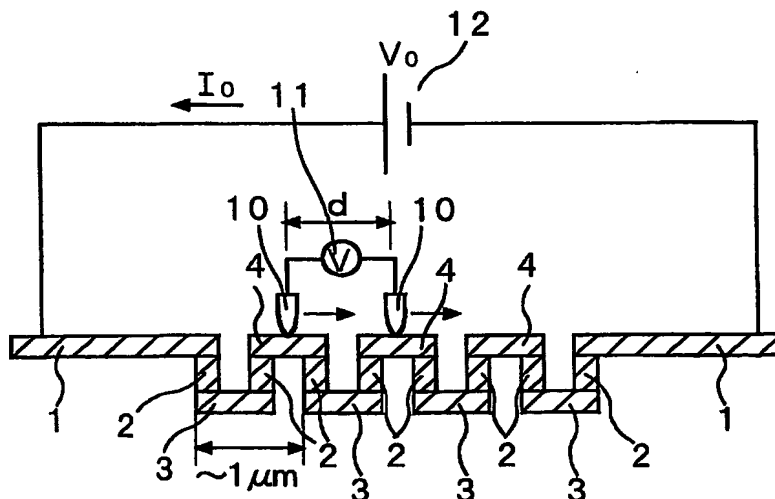
(30) Priority Data:
2003-289031 7 August 2003 (07.08.2003) JP

Published:
— with international search report
— before the expiration of the time limit for amending the
claims and to be republished in the event of receipt of
amendments

(71) Applicant (for all designated States except US): NEC
ELECTRONICS CORPORATION [JP/JP]; 1753
Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa
211-8668 (JP).

For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.

(54) Title: SCANNING PROBE INSPECTION APPARATUS



(57) Abstract: A pair of pads (1) are formed on an insulating layer formed on a top surface of a substrate, and a plurality of through- holes (2) are arranged laid out at equal intervals between the pads (1). The adjoining through holes (2) are connected alternately by upper-layer wireupper interconnect lines (4) exposed on the insulating layer or lower-layer wirelower interconnect lines (3) buried in the insulating layer, thus constituting a check pattern. A DC power supply (12) is connected between the pair of pads (1), and a constant current I_0 is supplied to a chain pattern of the through holes (2). Two probes

(10) move on a chip surface along the chain pattern of the through holes (2) while keeping a given interval spacing d . Accordingly, the probes (10) sequentially scan the upper-layer wireupper interconnect lines (4) exposed through the chip surface of the chain pattern of the through- holes (2).